REMARKS

In view of the amendments proposed above, Applicants respectfully request consideration of the following remarks.

Anticipation Rejections Under 35 U.S.C. § 102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Anticipation Rejection Based on United States Patent Application Publication US 2002/0199052 to Moyer

Claims 1-41 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent Application Publication 2002/0199052 to Moyer (hereinafter "Moyer"). Applicants respectfully traverse this rejection as set forth below.

Moyer discloses a bus arbitration scheme for the global bus of a computer system that includes – in addition to the global bus (see FIG. 1, item 12) – a CPU 14, system memory 20, 22, 24, alternate bus masters 36, 38, 40, peripherals 28, 30, and a bus arbiter 34, all coupled with the global bus 12. Moyer, at paragraphs 0017 and 0022 (lines 1-3). The bus arbiter 34 includes (see FIG. 4) a Logic Circuit 50 coupled with the global bus 12 to receive Current Transfer Type Signals 53. Moyer, at paragraph 0021. Bus arbiter 34 also includes a Policy Select Logic circuit 54 coupled with Logic Circuit 50, wherein

the Policy Select Logic circuit 54 generates an Arbitration Policy signal that is connected to an input of Logic Circuit 50. Moyer, at paragraph 0021. Moyer goes on to state:

> Bus Arbiter 34 uses **information about a current transfer** to make Global Bus 12 control decisions upon receipt of one or more bus requests to use Global Bus 12. When Logic Circuit 50 receives one or more bus requests from any of CPU 14 and Alternate Bus Masters 36, 38, and 40, a decision is made within Logic Circuit 50 **based upon some predetermined criteria** as to which bus request should be serviced first.
>
> * * * *
>
> Logic Circuit 50 conditionally asserts the Bus Grant CPU signal or a Bus Grant signal for one of the requesting Alternate Bus Masters 36, 38, and 40 **based on the Current Transfer Type Signals** 53 and **information contained in Control Register** 56. If bus ownership is transferred to a master other than the one performing the current transfer (i.e. transfer master status from a present or current communication bus master), the current transfer is interrupted, and a previously asserted bus grant signal is negated in order to force the Global Bus 12 to be relinquished and thus allow the higher priority master to gain bus ownership during an on-going burst transfer. Moyer, at paragraph 0022 (emphasis added).

Thus, Moyer discloses a bus arbitration scheme, wherein bus ownership is assigned based upon: (1) information about the transfer currently taking place on the global bus; and (2) some predetermined arbitration policy. In the arbitration scheme disclosed in Moyer, **ownership is not transferred in response to detection of a reserved memory address**.

In contrast to Moyer, claim 1 of the present application, as amended herein, recites a method including the following limitations:

> 1. A method comprising:
>
> initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;
>
> monitoring signals on the memory bus;
>
> detecting a first sequence of signals, the first sequence of signals including **a reserved memory address**; and
>
> switching control of the at least one memory element to the circuit in response to detection of **the reserved memory address**.

Each of independent claims 11 and 20, as amended, as well as independent claim 36, recites some limitations similar to those recited in claim 1 above. The claim amendments proposed herein, as well as new claims 30-43, find support in the as-filed specification at paragraphs 0020 through 0033, notably paragraphs 0023 and 0028-0031.

Thus, the present claimed invention is directed to a scheme wherein a memory bus is monitored for a sequence of signals that includes a reserved memory address. If the reserved memory address is detected on the memory bus, control of a memory is switched from one processing unit to another in response to the detection of this signal sequence that includes the reserved memory address. The reserved memory address corresponds to an address in a reserved portion of the memory (or another memory). Each of claims 1, 11, and 20 was amended to clarify that **control of the memory is switched in response to detection of the reserved memory address**. Moyer does not disclose this method of switching control of a memory between two separate processing units.

Accordingly, as Moyer fails to teach at least the above-noted limitations of each of independent claims 1, 11, 20, and 36, each of these claims is novel in view of Moyer. Also, claims 2-10, 30, and 31, claims 12-19, 32, and 33, claims 21-29, 34, and 35, and claims 37-41 are allowable as depending from novel independent claims 1, 11, 20, and 36 respectively.

In rejecting claim 36, regarding the limitation of "the reserved memory address," the Examiner states that "the reserved memory address is *any* address corresponding to memory elements 20, 22 and 24 in Figure 1." Office Action, at page 5. This interpretation of the claim limitation "reserved memory address" is inconsistent with the as-filed specification, where it is stated that the "reserved memory addresses are memory addresses that are set aside by the processing element device driver software so as to either enable the switching of local memory bus 355 or to commence the initializing of processing element 300." Specification, at 0029. Thus, the Applicants respectfully assert that the Examiner has accorded an unreasonably broad interpretation to the claim limitation of a "reserved memory address" that is not consistent with the specification.

See *In re Morris*, 44 U.S.P.Q.2d 1023, 1027 (Fed. Cir. 1997) (stating that "it would be unreasonable for the PTO to ignore any interpretive guidance afforded by the applicant's written description"); *Rowe v. Dror*, 42 U.S.P.Q.2d 1550, 1555 (Fed. Cir. 1997) (stating that "claims receive their broadest reasonable meaning" during the examination process, but this "does not relieve the PTO of its essential task of examining the entire patent disclosure to discern the meaning of claims words and phrases"); and *In re Sneed and Young*, 218 U.S.P.Q. 385, 388 (Fed. Cir. 1983) (stating that it "is axiomatic

that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation *consistent with* the specification") (emphasis added).

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations. M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on United States Patent Application Publication US 2002/0199052 to Moyer

Claims 42-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moyer. Applicants respectfully traverse this rejection as set forth below.

As set forth above, Moyer fails to disclose all limitations of independent claim 36 and, therefore, claim 36 is patentable in view of Moyer. If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. §2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 42 and 43 are allowable as depending from nonobvious, independent claim 36.

CONCLUSION

Applicants submit that claims 1-43 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, L.L.P.

Date: September 4, 2003

Kerry D. Tweet
Registration No. 45,959

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(503) 684-6200

KDT/acf